Claims

[c1] 1. A differential amplifier circuit comprising:
a first differential amplifier for receiving a pair of differential input signals to generate a first output;
a second differential amplifier for receiving said pair of differential input signals to generate a second output; and
a summing circuit for summing said first output of said first differential amplifier and said second output of said second differential amplifier to provide a common output for said differential amplifier circuit.

[c2] 2. The differential amplifier circuit of Claim 1, wherein said first differential amplifier is an n-channel differential amplifier.

[c3] 3. The differential amplifier circuit of Claim 2, wherein said first differential amplifier includes a pair of n-channel transistors for receiving said pair of differential input signals, respectively.

[c4] 4. The differential amplifier circuit of Claim 1, wherein said second differential amplifier is a p-channel differential amplifier.

[c5] 5. The differential amplifier circuit of Claim 1, wherein said second differential amplifier includes a pair of p-channel transistors for receiving said pair of differential input signals, respectively.

[c6] 6. The differential amplifier circuit of Claim 1, wherein said summing circuit is an n-channel differential amplifier.

[c7] 7. The differential amplifier circuit of Claim 5, wherein said summing circuit includes a pair of n-channel transistors for receiving a voltage reference signal and output signals from said first output of said first differential amplifier and said second output of said second differential amplifier.

[c8] 8. The differential amplifier circuit of Claim 6, wherein said differential circuit further includes a reference voltage generation circuit for providing said reference voltage for said summing circuit.

[c9] 9. The differential amplifier circuit of Claim 7, wherein said voltage reference circuit includes a differential amplifier having inputs connected to an output of said differential amplifier.

[c10] 10. The differential amplifier circuit of Claim 1, wherein

said first and second differential amplifiers receive an active low ENABLE_N signal.

[c11] 11. The differential amplifier circuit of Claim 9, wherein said summing circuit receives an active low ENABLE_P signal.

[c12] 12. The differential amplifier circuit of Claim 10, wherein said summing circuit includes a clamp device to hold said common output high when said ENABLE_P signal is low.

[c13] 13. The differential amplifier circuit of Claim 1, wherein said first differential amplifier receives a gate control voltage V_{CMN} to control the current through an n-channel transistor within said first differential amplifier in a consistent and predictable manner using a current mirror technique.

[c14] 14. The differential amplifier circuit of Claim 1, wherein said second differential amplifier receives a gate control voltage V_{CMP} to control the current through a p-channel transistor within said second differential amplifier in a consistent and predictable manner using a current mirror technique.

[c15] 15. The differential amplifier circuit of Claim 1, wherein said summing circuit receives a gate control voltage V_{CMN}

to control the current through an n-channel transistor within said summing circuit in a consistent and predictable manner using a current mirror technique.